IN THE SPECIFICATION

Please correct the paragraph at page 12, lines 6-18 as follows:

The input circuit of one example embodiment is comprised of resistors R1 and R2 having a value of 105K ohms and 81K ohms, which places approximately 2.2 volts onto the gate of transistor 402. Since transistor 401 is on, charging current I_{CHRG} flows to charge battery 202. In this example, the node between transistor 401 and 402 is one diode drop above the gate bias voltage of transistor 402 (approximately 3.0-4.5 volts). The parasitic source-to-Nwell diode 450 of transistor 402 operably establishes the floating well voltage at approximately one diode drop below the source voltage of transistor 402 (approximately 2.5-3.8 volts). The biasing conditions of transistor 402 ensures that no node-to-node potential (terminal-to-terminal voltage) on any single component exceed the maximum voltage the process may handle (or some specified value which is not to be exceeded). Note that R_{BIAS} is actually present in the circuit, but is not shown since ~~it's~~ its impedance is substantially higher than the other resistors which bias the gate of transistor 402.